CLAIMS

1. A semiconductor device comprising:

a drain region having a first conductivity type;

a body region formed above said drain region having a second conductivity type opposite said first conductivity type;

a source region of said first conductivity type formed in said body region so that said source region is separated from said drain region by said body regions;

an upward opening dielectric region lining a first upward opening rectangular groove extending downward through said source and said body regions and into said drain region so that a first portion of said source region and a first portion of said body region lie on one side of said rectangular groove and a second portion of said source region and a second portion of said body region lie on the other side of said rectangular groove, said upward opening dielectric region defining a second upward opening rectangular groove;

a gate region having a top surface, said gate region completely filling the bottom portion of said second upward opening rectangular groove, said top surface of said gate region being situated between said first portion and said second portion of said source region; and

an insulating region having a planar top surface formed above said gate region and above said first and said second portions of said source and said body regions.

2. A semiconductor device as in Claim 1 wherein said source and said body regions are formed in an epitaxial layer having said first conductivity type.

3. A semiconductor device as in Claim 1 wherein said

drain region comprises a semiconductor substrate, said body region consists of an epitaxial layer formed on said substrate, and said gate region extends into said substrate.

4. A semiconductor device as in Claim 1 wherein said drain region comprises a semiconductor substrate and a selected portion of an epitaxial layer formed on said semiconductor substrate and said gate region extends through said epitaxial portion of said drain region into said substrate.

5. A semiconductor device as in Claim 1 further including a fourth region having said second conductivity type, said fourth region underlying said drain region, said first portion of said body region, said drain region, and said fourth region comprising an emitter, base, and collector, respectively, of a junction transistor.

6. A semiconductor device comprising:

a block of semiconductor material having a top surface;

an upward opening dielectric region lining an upward opening rectangular groove extending downward from said top surface into said block of semiconductor material, said upward opening dielectric region thereby defining a second upward opening rectangular groove;

a source region of first conductivity type extending downward into said block of semiconductor material from said top surface adjacent a first portion of said dielectric region;

a body region of second conductivity type opposite said first conductivity type in said block of semiconductor material, said body region underlying and being adjacent said source region and being adjacent a second portion of said dielectric region;

a drain region of said first conductivity type in said block of semiconductor material, said drain region

being adjacent and underlying said body region and being adjacent a third portion of said dielectric region;

a gate region having a top surface, said gate region completely filling the bottom portion of said second upward opening rectangular groove, said top surface of said gate region being opposite said source region; and

an insulating material having a planar top surface formed above said gate region and above said source region.

7. A semiconductor device as in Claim 6 further comprising a region of said second conductivity type underlying said drain region, wherein

a portion of said body region, a portion of said drain region and a portion of said region of said second conductivity type underlying said drain region comprise a junction transistor.

8. A method of making a semiconductor device comprising the following steps:

forming a first region of a semiconductor material having a first conductivity type;

forming a second region of a semiconductor material having a second conductivity type above and in contact with said first region, said second region having a top surface;

forming a third region of said first conductivity type in a first portion of said second region, said third region extending to a first portion of said top surface;

forming a first rectangular groove in said first portion of said top surface, said rectangular groove extending downward through said third and said second regions into said first region so that a first portion of said third region and a first portion of said second region lie on one side of said rectangular groove and a

second portion of said third region and a second portion of said second region lie on the other side of said rectangular groove;

lining said rectangular groove with a dielectric material thereby forming a second, inner rectangular groove;

filling the bottom portion of said second, inner rectangular groove with a conductive material so that a top surface of said conductive material in said second groove lies between said first portion and said second portion of said third region;

forming an insulating layer having a planar top surface over the device resulting from the preceding steps.

9. A method as in Claim 8 wherein said first region is formed on a fourth region of semiconductor material of said second conductivity type.

10. A method of making a semiconductor device comprising the following steps:

forming a first region of a semiconductor material having a first conductivity type;

forming a second region of a semiconductor material having a second conductivity type above and in contact with said first region, said second region having a top surface;

forming a third region of said first conductivity type in a first portion of said second region, said third region extending to a first portion of said top surface;

forming a first rectangular groove in said top surface, said groove extending downward into said first region so that a portion of said third region and a portion of said second region lies adjacent said groove on one side of said groove;

lining said groove with a dielectric material thereby forming a second, inner rectangular groove;

filling the bottom portion of said second, inner

rectangular groove with a conductive material so that a top surface of said conductive material in said second groove lies opposite said portion of said third region;

forming an insulating layer having a planar top surface over the device resulting from the preceding steps.

11. A method as in Claim 10 wherein said first region is formed on a fourth region of semiconductor material of said second conductivity type.